

WHAT IS CLAIMED IS:

1. A data processor comprising:
a processor;
5 a first storage device; and
a second storage device connected between said processor and said first storage device,
wherein when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second
10 storage device, including said predetermined data, are read from said first storage device and transferred to a certain line of said second storage device by burst transfer,
whereby when an interrupt request occurs during said burst transfer, said burst transfer is suspended and an interrupt processing is started.
- 15 2. The data processor according to claim 1 wherein
said burst transfer suspended is restarted after the completion of said interrupt processing.
- 20 3. The data processor according to claim 2 wherein
said burst transfer suspended is restarted only when returning to the original program in which said burst transfer is suspended.
4. The data processor according to claim 2 wherein
when a plurality of interrupt requests occur, a plurality of interrupt processing
25 are executed sequentially and, after the completion of the last interrupt processing, said

burst transfer suspended is restarted.

5. The data processor according to claim 2, further comprising:

an information register for keeping information about a point at which said

5 burst transfer is suspended, wherein

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted.

10 6. The data processor according to claim 2 wherein

said second storage device has a plurality of lines,

each line having information about a point at which said burst transfer is suspended, and

among said plurality of data, only data not read from said first storage device
15 due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said burst transfer restarted.

7. The data processor according to claim 1 wherein

said burst transfer suspended is restarted when a certain line related to
20 suspension of said burst transfer is accessed by said processor after said interrupt processing is completed.

8. The data processor according to claim 7, further comprising:

an information register for keeping information about a point at which said

25 burst transfer is suspended, wherein

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said burst transfer restarted.

5 9. The data processor according to claim 7 wherein
said second storage device has a plurality of lines,
each line having information about a point at which said burst transfer is
suspended, and

 among said plurality of data, only data not read from said first storage device
10 due to suspension of said burst transfer are read from said first storage device and
transferred based on said information in said burst transfer restarted.

 10. The data processor according to claim 1 wherein
said burst transfer suspended is restarted when an instruction for terminating
15 said interrupt processing is detected during execution of said interrupt processing.

 11. The data processor according to claim 10 wherein
when a plurality of interrupt requests occur, a plurality of interrupt processing
are executed sequentially and, when an instruction for terminating the last interrupt
20 processing is detected, said burst transfer is restarted.

 12. The data processor according to claim 10, further comprising:
an information register for keeping information about a point at which said
burst transfer is suspended, wherein
25 among said plurality of data, only data not read from said first storage device

due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said burst transfer restarted.

13. The data processor according to claim 10 wherein
5 said second storage device has a plurality of lines,
each line having information about a point at which said burst transfer is
suspended, and
among said plurality of data, only data not read from said first storage device
due to suspension of said burst transfer are read from said first storage device and
10 transferred based on said information in said burst transfer restarted.

14. The data processor according to claim 1, further comprising:
a register to which a predetermined priority related to an interrupt factor is set,
and
15 a judgment unit comparing a priority of said interrupt request with said
predetermined priority set in said register, and judging, from the comparison result,
whether said burst transfer is suspended or not.

15. The data processor according to claim 1, further comprising:
20 a register to which permission or non-permission to suspend said burst transfer
is set for each interrupt factor,
wherein said burst transfer is suspended only when said interrupt request has an
interrupt factor that is set so as to permit suspension of said burst transfer.

25 16. The data processor according to claim 1 wherein

said interrupt instruction is executed after executing an instruction that is already fetched before an interrupt instruction corresponding to said interrupt request is fetched.

5 17. The data processor according to claim 1, wherein

instructions are processed in a pipeline having an instruction fetch stage
fetching the instructions,

a decode stage decoding the instructions fetched by the instruction fetch stage
and

10 an instruction execution stage executing the instructions decoded by the
decoded stage, wherein

an interrupt process is performed when said interrupt request occurs, and

first and second processes are selectively performed in accordance with a
priority of said interrupt request as the interrupt process,

15 said first process including a process that said instruction execution stage
executing an interrupt instruction corresponding to said interrupt request after executing
an instruction that is already fetched before the interrupt instruction is fetched by the
instruction fetch stage, and

20 said second process including a process that said instruction stage executing the
interrupt instruction before executing an instruction that is already fetched before the
interrupt instruction is fetched by the instruction fetch stage and that is not yet executed
by the instruction execution stage.

18. The data processor according to claim 17, further comprising:

25 a register to which a predetermined priority is set, and

a judgment unit comparing the priority of said interrupt request with the predetermined priority set in said register, and judging, from the comparison result, whether said first or second process is performed.

5 19. A data processor comprising:

a processor;

a first storage device; and

a second storage device connected between said processor and said first storage device,

10 wherein when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second storage device, including said predetermined data, are read from said first storage device and transferred to a certain line of said second storage device by burst transfer,

 and when a first branch instruction is detected during a first burst transfer in the
15 process of executing a first program, said first burst transfer is suspended and a second program as a branch target is executed,

 said data processor further comprising a register for keeping a first information about a point at which said first burst transfer is suspended, wherein

 upon completion of execution of said second program, said first burst transfer
20 suspended is restarted based on said first information.

20. The data processor according to claim 19 wherein,

 when a second branch instruction is detected during a second burst transfer in the process of executing said second program, said second burst transfer is suspended and
25 a third program as a branch target is executed,

said data processor further comprising another register for keeping a second information about a point at which said second burst transfer is suspended, wherein

upon completion of execution of said third program, said second burst transfer suspended is restarted based on said second information.